

In the specification:

[4] Hence, there is a need in the art for a means by which RAM failures may be readily diagnosed immediately after failure occurs, even while the integrated circuit is engaged in processing data flows in the field. One or more embodiments of the present invention addresses such needs.

SUMMARY OF THE INVENTION

[5] In accordance with one ~~aspect~~ embodiment of the present invention, a diagnostic read circuit transfers the content of any RAM imbedded in an integrated circuit and delivers the entire contents external to the integrated circuit for examination. Data can be delivered through a scan chain, dedicated external pins or internal buses that then go through external pins. The diagnostic read circuit can share any number of pins to be enabled and to deliver data externally. The diagnostic read circuit may include an address generator to ensure all RAM data contents are read, a data register for temporarily storing RAM data contents until ready to be delivered externally, and a sequence controller to initiate and control a RAM diagnostic read.

[6] In accordance with further ~~aspects~~ embodiments of the present invention, ~~the invention provides an integrated circuit comprising~~ a random access memory, and a diagnostic read circuit, either stand alone or imbedded in a built-in self-test circuit, that reads memory storage errors in the random access memory and provides random access memory data contents externally when a memory storage error is detected in the random access memory.

[7] In accordance with another ~~aspect~~ embodiment of the present invention, the diagnostic read circuit may be imbedded in a BIST and share the address generator and data register.

[9] In accordance with other ~~aspects~~ embodiments of the invention, an address generator provides data storage addresses to the random access memory for the fetching of the stored data. The fetched data and the data storage addresses are provided from the integrated circuit for external analysis responsive to a detected error in data storage. The data storage addresses may be transferred external to

the integrated circuit through, for example, a scan chain, external pin or pins, or an external bus.

[10] In accordance with a further ~~aspect~~embodiment of the present invention, ~~the invention provides, in an integrated circuit,~~performs a method to allow a read of a RAM at any time and to provide~~ing~~ the read memory contents for external analysis.

BRIEF DESCRIPTION OF THE DRAWINGS

[11] The foregoing aspects and many of the attended advantages of this invention will become more readily appreciated as the same become better understood by reference to the following non-limiting detailed description, when taken in conjunction with the accompanying drawings, wherein:

[14] **FIG. 3** is a block diagram of the BIST circuit of **FIG. 1** embodying the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[22] As will be noted in **FIG. 1** and **FIG. 3**, the BIST circuit **100** may provide read and write data storage and retrieval addresses to the RAMs **14** thru **16** over address bus **30**. In addition, the BIST **18** may provide preset data to the RAMs **14** thru **16** over data input bus ~~38~~32 and reads data from the RAMs **14** thru **16** over data bus **36**. As will be noted in **FIG. 3**, the BIST circuit **18** also includes the BIST sequence controller **150**, a data generator **56**, and a comparator **58**.